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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,324	12/04/2003	Debendra Mallik	P16831	7342

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,324	MALLIK ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/16/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10,15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,15 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed 12/19/2006 in response to the Office action mailed on 07/27/2006 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 2, 4-10, 15 and 17-19.

Claim Rejections - 35 USC § 103

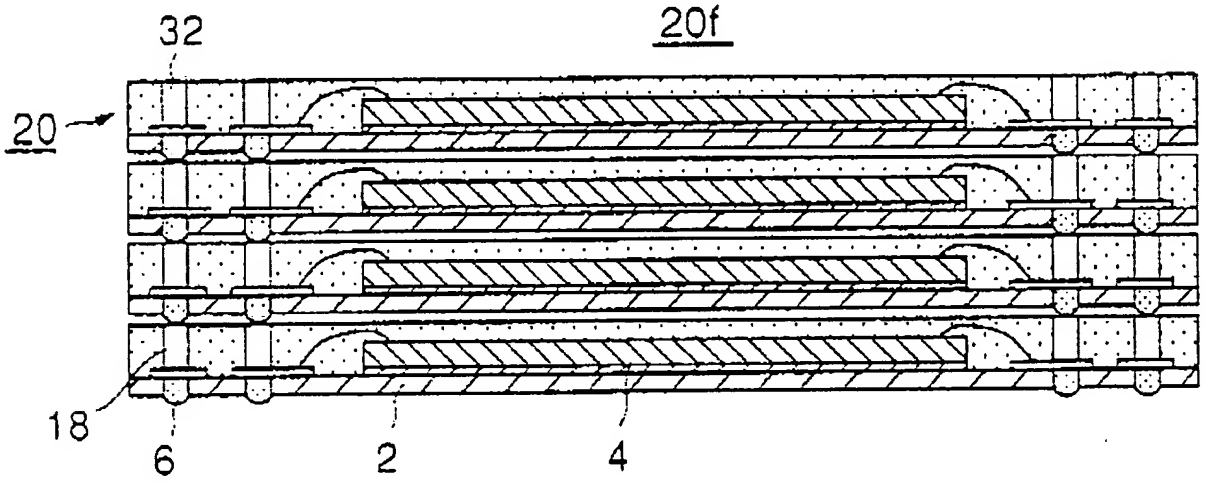
2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4-9 as being unpatentable over Taniguchi et al. (US 6,489,676 previously cited) in view of Lee (US 7,145,225)

4. Regarding claim 1, Taniguchi (e.g. figs. 9 and 12) shows an apparatus comprising: a first integrated circuit die 4; a first integrated circuit package 2 connected to the first integrated circuit die; mold compound 8 in contact with the first integrated circuit die and the first integrated circuit package; a first interconnect 6/10/18 in contact with the first integrated circuit package; a second integrated circuit package 2; a second interconnect 10/18/6 in contact to the second integrated circuit package, wherein a first portion 18 of the first interconnect is in contact with the mold compound, wherein a second portion 6 of the first interconnect is not in contact with the mold compound,

wherein the mold defines an opening, and wherein a third portion 10 of the first interconnect is in contact with the first integrated circuit package, and the second interconnect is in contact with the first interconnect.



Taniguchi does not shows that the second interconnect is in contact with the first interconnect within the opening. However, Lee (e.g. fig. 3) shows an interconnect having a first interconnect (2/15/16/34) and a second interconnect (2/15/16/34) wherein tie second interconnect is in contact with the first interconnect within the opening. This limitation has been interpreted in light of the specification as a solder ball partially located within an opening in contact with a pad of an upper circuit package. In this case, the solder ball 34 is analogous to the ball 21 described in figure 1 of the instant invention.

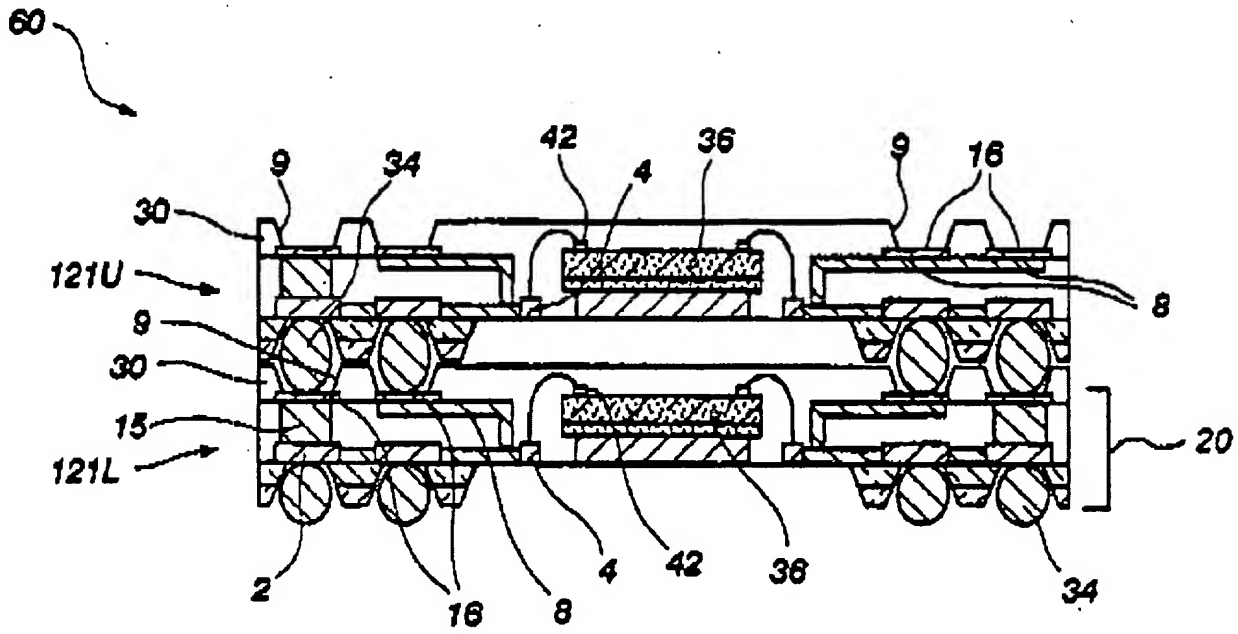


Fig. 3

It would have been obvious to one of ordinary skill in the art at the time the invention was made connect the second interconnect the first interconnect disclosed by Taniguchi within the opening to make a package having a reduced thickness as taught by Lee (see col. 3/lls. 17-40).

5. Regarding claim 2, Taniguchi shows the second portion is an upper portion of the interconnect and the third portion is a lower portion of the interconnect.

6. Regarding claim 4, Taniguchi shows a the second integrated circuit package is coupled to the mold compound (thermally).

7. Regarding claim 5, Taniguchi shows a second integrated circuit die 4 in contact with the second integrated circuit package 2; second mold compound 8 in contact with the second integrated circuit die and the second integrated circuit package; and a third

interconnect 18a connected with the second integrated circuit package, wherein a first portion (side surface) of the third interconnect is in contact with the second mold compound, and wherein a second portion (top surface) of the third interconnect is not in contact with the second mold compound, wherein the second mold compound defines a second opening, wherein the second portion of the third interconnection is recessed beneath the second opening, and wherein a third portion (bottom surface) of the third interconnect is in contact with the second integrated circuit package.

8. Regarding claim 6, Taniguchi shows a third integrated circuit package 2 (third package in upward direction); a fourth interconnect 18b coupled to the third integrated circuit package, wherein the fourth interconnect is coupled to the third interconnect (electrically).

9. Regarding claim 7, Taniguchi (e.g. fig. 18) shows a second integrated circuit 4a coupled to the integrated circuit die, in contact with the mold compound, and electrically coupled to the integrated circuit package.

10. Regarding claim 8 (as understood), Taniguchi (e.g. figs. 9 and 12) shows an apparatus comprising: a first integrated circuit package substrate 2; a plurality of integrated circuit dies (4/4a) coupled to the first integrated circuit package substrate (e.g. thermally, electrically); a mold compound 8 in contact with the integrated circuit die and the first integrated circuit package; a first interconnect 6/10/18 in contact with the first integrated circuit package substrate and electrically connected to one of the plurality of integrated circuits dies, a second integrated circuit package substrate 2; a second interconnect 6/10/18 in contact to the second integrated circuit package

substrate, wherein a first portion 18 of the first interconnect is in contact with the mold compound, wherein a second portion 6 of the first interconnect is not in contact with the mold compound, the mold compound defining an opening, and wherein a third portion 10 of the first interconnect is in contact with the first integrated circuit package and the second interconnect is in contact with the first interconnect. Taniguchi does not show that the second portion of the first interconnect is recessed beneath the opening and wherein the first and second interconnect are connected within the opening. However, Lee (e.g. fig. 3) shows an interconnect having a first interconnect (2/15/16/34) and a second interconnect (2/15/16/34) wherein the second portion 34 of the first interconnect is recessed beneath the opening. Also, shows that the first and second interconnect are in contact within the opening. This limitation has been interpreted in light of the specification as a solder ball partially located within an opening in contact with a pad of an upper circuit package. In this case, the solder ball 34 is analogous to the ball 21 described in figure 1 of the instant invention. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second portion of the first interconnect disclosed by Taniguchi recessed beneath the opening and to connect the first and second interconnects within the opening to make a package having a reduced thickness as taught by Lee (see col. 3/lls. 17-40).

11. Regarding claim 9, Taniguchi shows a die attach material disposed between the first faces of each of the plurality of circuit package substrate (col. 1/lls. 43).

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. (US 6,489,676 previously cited) in view of Lee (US 7,145,225) in view of Takiar (US 5,422,435 previously cited).

13. Regarding clam 10, Taniguchi in view of Lee shows most aspects of the instant invention except for a second integrated circuit in contact to the first integrated circuit die 4, in contact with the mold compound, and electrically couple the integrated circuit package. Takiar (e.g. fig. 8) shows a package comprising a stacked arrangement of semiconductor dies that provide a single circuit assembly. As shown in figure 5, a second integrated circuit die 174 is coupled to a first integrated circuit die 172 is in contact with the mold compound 25 (e.g. fig. 1), and is electrically couple the integrated circuit package 182. According to Takiar, this type of arrangement is used to decrease the size and weight of the device, as well as to improve its performance (col. 2/lls. 3-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device disclosed by Taniguchi in view of Lee having two or more semiconductor dies wherein the second integrated circuit die is coupled to the first integrated circuit die, in contact with the mold compound, and electrically couple the integrated circuit package in order to provide a single circuit assembly having a decreased size and weight as suggested by Takiar.

14. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. (US 6,489,676 previously cited) in view of Lee (US 7,145,225) further in view of Chang (US 20020196650; previously cited).

15. Regarding claim 15, Taniguchi (e.g. figs. 9 and 12) shows a system comprising: a first integrated circuit die 4; a first integrated circuit package 2 in contact with the first integrated circuit die; a mold compound 8 in contact with the first integrated circuit die and the first integrated circuit package; a first interconnect 06/10/18 in contact with the first integrated circuit package; a second integrated circuit die 4; second integrated circuit package 2 (e.g. fig. 12); a second interconnect 6/10/18 in contact to the second integrated circuit package, wherein a first portion 18 of the first interconnect is in contact with the mold compound, wherein a second portion 6 of the first interconnect is not in contact with the mold compound, wherein the mold compound defines an opening and wherein a third portion 10 of the first interconnect is in contact with the first integrated circuit package. Taniguchi does not show that the system includes a double data rate memory and that the second portion of the first interconnect is recessed beneath the opening and wherein the first and second interconnect are connected within the opening. However, Chang teaches (e.g. fig. 2) a computer system including a double data rate memory (204-207) electrically coupled to an integrated circuit die 202. Chang teaches that under the mode of double data rate, the memory can perform data access control during both the raising edge and falling edge of the system clock signal. Thus, the operation speed of the memory is fastened (pps. 005, 006 & 0028). Furthermore, Lee (e.g. fig. 3) shows an interconnect having a first interconnect (2/15/16/34) and a second interconnect (2/15/16/34) wherein the second portion 34 of the first interconnect is recessed beneath the opening. Also, shows that the first and second interconnect are in contact within the opening. According to Lee this

embodiment provide a package having a reduced thickness (see col. 3/lls. 17-40). This limitation has been interpreted in light of the specification as a solder ball partially located within an opening in contact with a pad of an upper circuit package. In this case, the solder ball 34 is analogous to the ball 21 described in figure 1 of the instant invention. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second portion of the first interconnect disclosed by Taniguchi recessed beneath the opening and to connect the first and second interconnects within the opening to make a package having a reduced thickness as taught by Lee and to electrically couple a double data rate memory to the integrated circuit die disclosed by Taniguchi in view of Lee in order to increase the operation speed of the system as suggested by Chang.

16. Regarding claim 16, Taniguchi shows a second integrated circuit die 4 coupled to a second integrated circuit package 2; second mold compound 8 in contact with the second integrated circuit die and the second integrated circuit package; and a second interconnect 18a coupled to the second integrated circuit package and the first interconnect within the opening.

17. Regarding claim 17, Taniguchi shows that the second circuit package in coupled to the mold compound (i.e. thermally).

18. Regarding claim 18, Taniguchi (e.g. fig. 18) shows a second integrated circuit 4a coupled to the first integrated circuit die, in contact with the mold compound, and electrically coupled to the integrated circuit package.

19. Regarding claim 19, Chang shows a mother board 200 electrically coupled to the integrated circuit die and to the memory.

Response to Arguments

20. Applicant's arguments with respect to claims 1, 2, 4-10, 15 and 17-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andújar
Primary Examiner
Art Unit 2826

01/05/2007